ESSDERC
IEEE 51st European Solid-State Device Research Conference

JOINT PLENARY talks live broadcast:
September 13, 2021

ESSDERC KEYNOTE talks live broadcast:
September 15, 2021

LIVE Q&A INTERACTIVE sessions for all Conference Technical sessions: September 14-16-17, 2021
(on demand videos available from September 6 until November 30, 2021) All times are CEST

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At ST, we are 46,000 creators and makers of semiconductor technologies mastering the semiconductor supply chain with state-of-the-art manufacturing facilities. An independent device manufacturer, we work with our 100,000 customers and thousands of partners to design and build products, solutions, and ecosystems that address their challenges and opportunities, and the need to support a more sustainable world. Our technologies enable smarter mobility, more efficient power and energy management, and the wide-scale deployment of the Internet of Things and 5G technology. Further information can be found at www.st.com
SK hynix is a multinational company with over three decades of expertise in semiconductor manufacturing. The company’s global presence spans from four production sites in Korea and China (Icheon, Cheongju, Wuxi, and Chongqing) to four R&D centers and ten sales offices across the world. Building on its existing technological prowess, SK hynix is making relentless R&D efforts and investments to develop cutting-edge technology and cost-competitive products to attain leadership in the global semiconductor market.

SK hynix mainly produces memory semiconductors such as DRAM and NAND flash that are essential components of various IT devices such as mobile and computing products, but the company’s portfolio also includes system semiconductors such as CMOS image sensors. Ever since the first pilot production of Korea’s very first 16Kb SRAM in 1984, SK hynix has been reinforcing its technological leadership by introducing a series of world’s first, smallest, fastest, and lowest-power innovations in the semiconductor industry.
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On behalf of the Organizing and Steering Committees, it is our pleasure to welcome you to the 51st IEEE European Solid-State Device Research Conference (ESSDERC) and the 47th IEEE European Solid-State Circuits Conference (ESSCIRC) 2021. The conference is proudly co-organized by CEA-Leti, STMicroelectronics, Soitec, Université Grenoble Alpes and Grenoble National Polytechnics Institute. We thank the IEEE Solid-State Circuits Society (SSCS) and the IEEE Electron Devices Society (EDS), as our conferences are fully sponsored by these two prestigious societies.

Due to sanitary uncertainties and constraints, and in order to comply with the organizing companies and university policies preserving the health of their employees and guests, we have to adopt a full virtual format.

ESSDERC-ESSCIRC visits again virtually Grenoble city, the core of the French Alps center of semiconductor.

Known as the birthplace of microelectronics in France, Grenoble Alpes has also shown itself to be a leader in digital technologies (computer science, artificial intelligence, connected objects and more...). The combination of skills in both hardware and software – a rarity in a single metropolitan area – has provided local stakeholders with an exceptional set of tools for innovation (Grenoble was ranked 5th most innovative city in the world by Forbes).

The tech industry encompasses over 41,500 jobs (more than 60% in semiconductor companies), all concentrated within a radius of 20km. The industry includes a diversity of companies, from innovative startups all the way up to leading multi-nationals. Several semiconductor companies have major R&D facilities in Grenoble, with notably STMicroelectronics for digital technology platforms and chip architecture and design and Soitec, covering, substrate, device and advanced design engineering. Moreover, Grenoble is home to an exceptional set of imaging actors: Apple (imaging design center), Prophesee (neuromorphic vision systems), STMicroelectronics (image sensors), Lynred (infrared detectors), E2V/Teledyne (technology systems and components), Xenocs (X-ray optics, X-ray sources and SAXS systems), Trixell (digital X-ray imaging), Pyxalis (design services and custom solutions development for advanced CMOS image sensors), etc.

5,300 highly skilled researchers are based in research laboratories in Grenoble area. The leading laboratory in the domain is the Laboratory for Electronics and Information Technology (CEA-Leti), pioneer in micro and nanotechnologies and an integral part of the CEA – France’s largest public research institution. All public laboratories linked to CEA, CNRS, Grenoble Polytechnics Institute (G-INP) and Universities are networked within University Grenoble Alps. In 2020, Université Grenoble Alpes (56,000 students and 80 laboratories), made its entry into the top 100 of the prestigious Shanghai Global Ranking, which compares the research productivity of the world’s top 1,000 universities. UGA is the only French university outside Paris to appear in the top 100.

At STMicroelectronics (ST), our diamond sponsor, 46,000 creators and makers of semiconductor technologies worldwide are mastering the
Chair’s Message

semiconductor supply chain with state-of-the-art manufacturing facilities. An independent device manufacturer, working with our 100,000 customers and thousands of partners to design and build products, solutions, and ecosystems that address their challenges and opportunities, and the need to support a more sustainable world. ST’s technologies enable smarter mobility, more efficient power and energy management, and the wide-scale deployment of the Internet of Things and 5G technology. ST commits to be carbon neutral by 2027.

Since 2003 both ESSDERC and ESSCIRC are running in parallel and have joint keynote speakers and joint focus sessions. The increasing level of integration for system-on-chip design made available by advances in semiconductor technology is calling for a deeper interaction among technologists, device experts, IC designers and system designers. As participant to ESSDERC and ESSCIRC, you not only have the opportunity to become familiar with the latest advances in these fields, but you will meet people who pioneered previous developments, you get access to enhance your international network in micro- and nano-electronics and you will be a witness to previews into emerging fields.

This year IEEE ESSDERC-ESSCIRC received a total of 301 submissions from 30 countries; 56.8% of the submissions came from Europe, 25.6% from Asia-Pacific and 15.9% from North America, clearly demonstrating the international character of the conference. We are very proud to announce that this level of submissions is very much similar to the one that we had for the 2019 Cracow edition, before any pandemic!

The conference has 3 plenary keynote speakers coming from STMicroelectronics, University of California, Berkeley and CEA-Leti, 3 ESSDERC plenary speakers coming from Georgia Institute of Technology, University of California and ISAE-SUPAERO Toulouse, 3 ESSCIRC plenary speakers coming from University of Toronto, Politecnico di Milano and Ulm University.

The selected papers are presented in 58 sessions. We are serving the 3 ESSDERC specific tracks, the 7 ESSCIRC specific tracks and the 3 joint ESSCIRC-ESSDERC tracks. This year, we are also showing in specific sessions the IEEE journal papers that took the place of ESSCIRC-ESSDERC2020 for the regular papers: the SSC-Letters special edition ESSCIRC, and the TED-brief special edition ESSDERC. 50 of such papers will be presented also during ESSCIRC-ESSDERC 2021.

We have also put in place a twinning operation with the Asian Solid-State Circuits Conference 2020, and 5 among their best papers will also be presented in a special session during ESSCIRC 2021. In exchange, 5 of our best papers will be as well presented during A-SSCC2021 next November.

We also thank all external sponsors for their support in this difficult time. We are very grateful to the excellent collaboration with the exceptional members of the Organizing Committee and the Technical Program Committee. A special place for our Conference Secretariat with Sistema Congressi, who accompany us since last year and have smoothly helped us to ensure the transition to a fully virtual conference. All members and subcontractors have been extremely devoted and have worked very hard to make ESSCIRC-ESSDERC 2021 yet another successful event.
Chair’s Message

out their dedication, enthusiasm and professionalism this would not have been possible. We also thank all collaborators and volunteers who have helped us out.

Enjoy the 2021 edition of ESSCIRC-ESSDERC and we hope that the virtual experience that we will offer will reflect our traditional conferences spirit. Please come and interact with authors and friends through the chat and numerous live events!

We hope to see you all again in person, in Milano, Italy, for IEEE ESSCIRC-ESSDERC 2022!

Thomas ERNST and Dominique THOMAS
Conference General Chairs – ESSDERC-ESSCIRC 2021
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Andreia CATHELIN and Sylvain CLERC
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3. TRACK Compact modeling and process/device simulation

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Sadayuki YOSHITOMI, Kioxia, JP
Zhiping YU, Tsinghua University, CN

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11. JOINT TRACK Emerging Computing Devices and Circuits
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Iuliana RADU, imec, BE
Bogdan STASZEWSKI, University Collage Dublin, IE
Andrei VLADIMIRESCU, UC Berkeley, US
Domenico ZITO, Aarhus University, DK

12. JOINT TRACK: Memory Devices and Circuits towards non Von Neumann
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Elisa VIANELLO, CEA-Leti, FR - ESSDERC Track Chair
Nitin CHAWLA, STMicroelectronics, IN
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Marian VERHELST, KUL, BE
Wen-Kuan YEH, Narlab, TW
Christian ZAMBELLI, Università di Ferrara, IT
13. JOINT TRACK: Devices and circuits for Sensors, Optoelectronics and Display

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Matthias KHUL, TU Hamburg, DE
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Minhao YANG, EPFL, CH
The aim of ESSDERC and ESSCIRC is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The increasing level of integration for system-on-chip design made available by advances in semiconductor technology is, more than ever before, calling for a deeper interaction among technologists, device experts, IC designers and system designers. While keeping separate Technical Program Committees, ESSDERC and ESSCIRC are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions, regardless to which conference they belong.

**ESSDERC 2021 Tracks**

- Advanced Technology, Process and Materials
- Analog, Power and RF Devices
- Compact modeling and process/device simulation

**ESSDERC/ESSCIRC 2021 JOINT Tracks**

- Emerging Computing Devices and Circuits
- Memory Devices and Circuits towards non Von Neumann
- Devices and Circuits for Sensors, Optoelectronics and Display

**ESSDERC 2021 Virtual Format**

**PREAMBLE WEEK:**

- Virtual platform will open on September 6, 2021.
- All regular Conference presentations will be available on demand. Access will end on November 30, 2021.

**INTERACTIVE CONFERENCE WEEK: September 13 - 17, 2021**

- Live broadcast of Joint plenary and Keynote presentations
- Live Q&A sessions for all other conference sessions

All times are CEST
JOINT PLENARY KEYNOTES

JOËL HARTMANN
Executive Vice President
Digital & Smart Power Technology and Digital Front-End Manufacturing
STMicroelectronics, France

Artificial Intelligence: Why Moving it to the Edge?
This keynote is describing the evolution of Artificial Intelligence (AI) adoption to the Edge for maximizing Data processing at the User experience level to treat as much as possible data analysis without saturating Internet traffic and Cloud data centers. Evolution of Neural Network (NN) computing through progressive usage of In Memory Computing (IMC) is also described. A few examples of Artificial Intelligence at the Edge are also commented. We then describe how at ST, we address competitive solutions for Edge AI thanks to differentiated FD-SOI CMOS technology, Phase Change Memory (PCM) embedded memory integration and advanced NN and IMC design solutions.

Joël Hartmann is Executive Vice President of STMicroelectronics, Digital & Smart Power Technology and Digital Front-End Manufacturing, and has held this position since February 2012. He manages ST’s manufacturing operations in Crolles and Rousset, France, Technology and Design Platforms for the Company’s digital products. In December 2018, Hartmann’s mandate was expanded with ST’s Smart Power Technology R&D operations in Agrate, Italy. From 1979 to 2000, Hartmann worked at CEA-Leti, France-based applied-research center. In 2000, he joined STMicroelectronics as Director of the Crolles2 Alliance, the semiconductor manufacturing R&D initiative of STMicroelectronics, NXP, and Freescale Semiconductor. In 2008, Hartmann was promoted to Group Vice President and Director of Advanced CMOS Logic & Derivative Technologies. From 2010 to 2012, he had additional responsibilities as a co-leader of the Semiconductor Research and Development Center in Fishkill, NY, within the IBM ISDA Technology Alliance for advanced CMOS process development. Hartmann is a Member of the IEEE Electron Device Society. In 2017, he became a member of the French "Académie des Technologies" and received the European SEMI Award in 2019. Hartmann has filed 15 patents on semiconductor technology and devices and authored 10 publications in this field to date. Joël Hartmann was born in Toulon, France, in 1955. He graduated from the Ecole Nationale Supérieure de Physique de Grenoble with a degree in Physics.
Overcoming the Data Deluge Challenges with Greener Electronics

The purpose of this paper is to propose scientific and technical directions to reach global data and power sobriety while preserving computational efficiency. We present nine opportunities to lower the power consumption of computing units. A growth factor of 100 to 1000 in energy efficiency is achievable in the next 10 years if we take full advantage of all the potential improvements, working simultaneously at all five levels of the technological ecosystem (process steps, circuits, architecture, software and algorithms).

Jean-René Lèquepeys was named CEA-Leti’s Vice-President and Director of Programs in January 2019, following more than 30 years of scientific and managerial leadership at both CEA and CEA-Leti. He joined CEA in 1985 in the detection and intrusion-detection laboratory in CEA’s central security department and was promoted to lab manager in 1987. He joined CEA-Leti in 1993 as an R&D engineer specializing in image processing and also worked on the institute’s telecom projects. He was named head of deployment of the Telecom, Communicating Objects and Smart Card programs in 1999 and was promoted to head of the Circuit Design Department of CEA-Leti in 2005. In that role, Jean-René created a research center in Gardanne (France), pioneering secured electronic components, in partnership with School of Mines of Saint-Etienne (France). In 2010, he started a new department specializing in electronic architectures, integrated circuit design and embedded software, bringing together CEA-Leti and CEA-List researchers. He also helped launch CEA-Leti’s Silicon Components Division in 2011 and was named head of the division in 2017. Jean-René returned to the Electronic Architectures, Integrated Circuit Design and Embedded Software Department in 2018 before taking his current position.

Jean-René graduated from Supélec (1983) and taught physics for two years in Ouarazzate, Morocco. In 2000, he won the “Grand Prix de l'électronique Général Ferrié” for his work in telecommunications. He holds approximately 15 patents in that field.
Architecting the Human Intranet

Equipping us humans with the necessary tools to interact with, survive, and prosper in a rapidly changing world may require us to intimately adopt some of the same technologies that are causing some of these changes. Various wearable devices have been or are being developed to do just that. To be effective, functionality cannot be centralized and needs to be distributed to capture the right information at the right place. This requires a human intranet, a platform that allows multiple distributed input/output and information processing functions to coalesce and form a single application. How to effectively do so in light of the many challenges from an efficiency, usability, and effectiveness perspective is the focus of this paper.

Jan M. Rabaey holds the Donald O. Pederson Distinguished Professorship at the University of California at Berkeley. He is a founding director of the Berkeley Wireless Research Center (BWRC) and the Berkeley Ubiquitous SwarmLab, and has been the the Electrical Engineering Division Chair at Berkeley twice. Prof. Rabaey has made high-impact contributions to a number of fields, including advanced wireless systems, low power integrated circuits, sensor networks, and ubiquitous computing. His current interests include the conception of the next-generation integrated wireless systems over a broad range of applications, as well as exploring the interaction between the cyber and the biological world. He is the recipient of major awards, amongst which the IEEE Mac Van Valkenburg Award, the European Design Automation Association (EDAA) Lifetime Achievement award, and the Semiconductor Industry Association (SIA) University Researcher Award. He is an IEEE Fellow, a member of the Royal Flemish Academy of Sciences and Arts of Belgium, and has received honoray doctorates from Lund (Sweden), Antwerp (Belgium) and Tampere (Finland). He has been involved in a broad variety of start-up ventures.
ESSDERC Keynote Speakers

PIERRE MAGNAN
Professor
Head of Image Sensor Group
ISAE-SUPAERO, France

The Essential Contribution of CMOS Imaging Technologies to Earth Observation Applications

In this paper we discuss how the high performances CMOS imaging process improvements, strongly driven by consumer market’s needs, has allowed this technologies to pop-up in the field of Earth Observation instruments traditionally making use of dedicated Charge Coupled Devices (CCD). After reviewing the various Earth image captures techniques and related sensor architectures, the specific requirements on the sensor process will be examined and it will be shown how modern CMOS imaging process, although developed initially for high volume small pixel pitch application, can efficiently fulfill these needs, even allow new performances level, and thanks to additional features enable new achievements particularly suited to the New Space context.

Pierre Magnan graduated in E.E. from University of Paris in 1980. After being a research scientist involved in analog and digital CMOS design up to from 1984 to 1993 in LAAS-CNRS, he moved in 1995 to image sensors research in SUPAERO, now called ISAE-SUPAERO, in Toulouse, France, where he was involved in active-pixels sensors research and development activities. Since 2002, he is Full Professor there and Head of Image Sensor Research Group involved in CMOS Image Sensor research in cooperation with European companies (including STMicroelectronics, Airbus Defense & Space, Thales Alenia Space and also European and French Space Agencies) and development of custom image sensor dedicated to space instruments.

He has supervised 20 PhDs candidates in the field of image sensors and co-authored more than 80 scientific papers. He has served in IEEE IEDM Display Sensors and MEMS subcommittee in 2011, 2012, and in the International Image Sensor Workshop (IISW) TPC in 2007, 2009, 2011, 2017, 2019 and 2021, being the General Technical Chair of 2015 IISW. He has been Associate Guest Editor of the IEEE TRANS. ELECTRON DEVICES for the Special Issue on Solid-State Image Sensors in 2009 and 2015.

His research interests include solid-state image sensors design, modeling, technology, hardening techniques and circuit design for imaging applications.
ESSDERC Keynote Speakers

MARK RODWELL
Doluca Family Endowed Chair and Professor
Electrical and Computer Engineering Department
University of California Santa Barbara, USA

Transistors for 100-300GHz Wireless
We examine the potential design and performance of 100-300 GHz wireless communications systems, examine the required transistors performance, and describe our present efforts to develop InP bipolar and field-effect transistors to serve in the transmitters and receivers of such systems.

Mark Rodwell holds the Doluca Family Endowed Chair and is Professor in the Electrical and Computer Engineering Department at UCSB. He received the 1994, 1997, 1998, 2014, 2019, 2020, and 2021 departmental teaching awards.
He directs the SRC/DARPA Center for Converged TeraHertz Communications and Sensing. From 2007-14 he directed the SRC Nonclassical CMOS Research Center. From 1996-2018 he directed the UCSB Nanofabrication Lab during its growth to a 500-user facility.
His research group works to extend the operation of electronics to the highest feasible frequencies. Their research thus includes semiconductor devices (diodes & transistors), semiconductor fabrication process, circuit design, interconnects, instruments, and communications systems. Particular interests include THz InP bipolar transistors, nm III-V MOSFETs for both VLSI and THz applications, IC design above 50 GHz in both III-V and Silicon VLSI technologies, and mm-wave wireless communications system design.

Prof. Rodwell received the 2010 IEEE Sarnoff Award and the 2009 IEEE IPRM Conference Award for the development of InP-based bipolar IC technology, at both the device and the circuit design levels, for mm-wave and sub-mm-wave applications. His group's work on GaAs Schottky-diode ICs for picosecond / mm-wave instrumentation was awarded the 1997 IEEE Microwave Prize and the 1998 European Microwave Conference Microwave Prize. His group's collaborative development, with Prof. Madhow's group, of mm-wave line-of-sight MIMO received the 2012 IEEE Marconi Prize Paper Award. Prof. Rodwell was elected IEEE Fellow in 2003.
Compute-in-Memory: from Device Innovation to 3D System Integration

Compute-in-memory (CIM) hardware accelerator has been emerged as a promising paradigm for executing the artificial intelligence (AI) tasks owing to its superior energy efficiency. In this keynote presentation, we survey recent progresses of CIM technologies from device-level demonstration to system-level benchmark. First, the ferroelectric devices (FeM-FinFET, ferroelectric non-volatile capacitor) are introduced for resistive and capacitive read-out mechanism for crossbar arrays. Second, resistive random access memory (RRAM) based CIM macro has been taped-out into prototype chips in commercial foundry process and the related NeuroSim validation with measured silicon data is shown. Last, heterogeneous 3D integration scheme for SRAM, RRAM and 3D NAND tiers and logic tier is proposed.

Shimeng Yu is currently an associate professor of electrical and computer engineering at Georgia Institute of Technology. He received the B.S. degree in microelectronics from Peking University in 2009, and the M.S. degree and Ph.D. degree in electrical engineering from Stanford University in 2011 and 2013, respectively. From 2013 to 2018, he was an assistant professor at Arizona State University.

Prof. Yu’s research interests are the semiconductor devices and integrated circuits for energy-efficient computing systems. His research expertise is on the emerging non-volatile memories for applications such as deep learning accelerator, in-memory computing, 3D integration, and hardware security. Among Prof. Yu’s honors, he was a recipient of NSF Faculty Early CAREER Award in 2016, IEEE Electron Devices Society (EDS) Early Career Award in 2017, ACM Special Interests Group on Design Automation (SIGDA) Outstanding New Faculty Award in 2018, Semiconductor Research Corporation (SRC) Young Faculty Award in 2019, ACM/IEEE Design Automation Conference (DAC) Under-40 Innovators Award in 2020, and IEEE Circuits and Systems Society (CASS) Distinguished Lecturer for 2021-2022, etc.

Prof. Yu served or is serving many premier conferences as technical program committee, including IEEE International Electron Devices Meeting (IEDM), IEEE Symposium on VLSI Technology, IEEE International Reliability Physics Symposium (IRPS), ACM/IEEE Design Automation Conference (DAC), ACM/IEEE Design, Automation & Test in Europe (DATE), ACM/IEEE International Conference on Computer-Aided-Design (ICCAD), etc. He is a senior member of the IEEE.
14:30 – OPENING WELCOME
Location: PLATINE Auditorium
Date: Monday, September 13
Thomas Ernst, ESSCIRC ESSDERC 2021 General Chair
Kenneth O, SSCS President
Ravi M. Todi, EDS President
Andreia Cathelin, ESSCIRC TPC Chair
François Andrieu, ESSDERC TPC Chair

A1L-1: JOINT Plenary 1
Chair(s): Andreia Cathelin; STMicroelectronics
Thomas Ernst; CEA-Leti, Grenoble
Location: PLATINE Auditorium
Date: Monday, September 13, 15:00 - 15:45
15:00 Artificial Intelligence: Why Moving It to the Edge?
Joël Hartmann, Paolo Cappelletti, Nitin Chawla, Franck Arnaud, Andreia Cathelin
STMicroelectronics, France

A2L-1: JOINT Plenary 2
Chair(s): Francois Andrieu; CEA-Leti
Dominique Thomas; STMicroelectronics
Location: PLATINE Auditorium
Date: Monday, September 13, 15:45 - 16:30
15:45 Overcoming the Data Deluge Challenges with Greener Electronics
Jean-René Léquepeys¹, Marc Duranton², Susana Bonnetier³, Sandrine Catrou⁴, Richard Fournel⁴, Thomas Ernst¹,
Laurent Hérault¹, Didier Louis¹, Ahmed Jerraya¹, Alexandre Valentin³, François Perruchot⁴, Thomas Signamarcheix¹,
Elisa Vianello¹, Carlo Reita¹
¹CEA-Leti, Université Grenoble Alpes, France; ²CEA-List, Paris-Saclay University, France; ³CEA-List, Université Grenoble Alpes, France

A3L-1: JOINT Plenary 3
Chair(s): Andreia Cathelin; STMicroelectronics
Francois Andrieu; CEA-Leti
Location: PLATINE Auditorium
Date: Monday, September 13, 16:30 - 17:15
16:30 Architecting the Human Intranet
Jan M. Rabaey, Ana Claudia Arias, Rikky Muller
University of California, Berkeley, United States

17:15 – PANEL DISCUSSION
**B1L-1: Imaging Arrays & Detectors**

**Chair(s):** Antoine Dupret; CEA  
Robert Henderson; *University of Edinburgh*

**Location:** PLATINE Auditorium

**Date:** Tuesday, September 14, 15:00 - 16:00

**15:00**  
*4.6μm Low Power Indirect Time-of-Flight Pixel Achieving 88.5% Demodulation Contrast at 200MHz for 0.54MPix Depth Camera*  
Cédric Tubert, Pascal Mellot, Yann Desprez, Céline Mas, Arnaud Authi, Laurent Simony, Grégory Bochet, Stéphane Droard, Jeremie Teysssier, Damien Miclo, Jean-Raphael Beza, Thibault Augey, Franck Hingant, Thomas Bouchet, Blainde Roig, Aurélien Mazar, Raoul Vergara, Gabriel Mugny, Arnaud Tournier, Frédéric Lalanne, Francois Roy, Boris Rodrigues Goncalves, Matteo Vignetti, Pascal Fonteneau, Vincent Farys, Francois Agut, Joao Miguel Melo Santos, David Hadden, Kevin Channon, Christopher Townsend, Bruce Rae, Sara Pellegrini  
STMicroelectronics, United Kingdom; STMicroelectronics, France

**15:12**  
*Advancements in Indirect Time of Flight Image Sensors in Front Side Illuminated CMOS*  
Markus Dielacher2, Martin Flatscher1, Reinhard Gabl1, Richard Gagg1, Dirk Offenberg1, Jens Prima3  
1Infineon Technologies AG, Germany; 2Infineon Technologies Austria AG, Austria; 3PMD Technologies AG, Germany

**15:24**  
*Dark Count Rate in Single-Photon Avalanche Diodes: Characterization and Modeling Study*  
Mathieu Sicrè3, Megan Agnew3, Christel Buix3, Jean Coignus1, Dominik Golanski3, Rémi Helleboid3, Bastien Mamdy3, Isobel Nicholson3, Sara Pellegrini3, Denis Rideau3, David Roy3, Francis Calmon2  
1CEA-Leti, France; 2INSA Lyon, France; 3STMicroelectronics, United Kingdom; 3STMicroelectronics, France

**15:36**  
*A High-Speed Low-Power Sun Sensor with Solar Cells and Continuous Operation*  
Rubén Gómez-Merchán, María López-Carmona, Juan Antonio Leñero-Bardallo, Ángel Rodríguez-Vázquez  
Universidad de Sevilla-IMSE-CNM CSIC, Spain

**15:48**  
*A 0.94-μVrms Input Noise Pixel-Level Continuous Time ΣΔ IADC Interface for THz Sensing*  
Gabriele Quarta1, Matteo Perenzi2, Stefano D’Amico2  
1Fondazione Bruno Kessler, Italy; 2Università Del Salento, Italy
B1L-5: RF Si-based Devices

Chair(s): Mikael Ostling; KTH Royal Institute of Technology in Stockholm
Frederic Allibert; SOITEC

Location: CHROME 1
Date: Tuesday, September 14, 15:00 - 16:00

15:00 High-Temperature Characterization of Novel Silicon-Based Substrate Solutions for RF-IC Applications
Quentin Courte, Martin Rack, Massinissa Nabet, Pieter Cardinael, Jean-Pierre Raskin
Université Catholique de Louvain, Belgium

15:12 Dual-Layer Proton Irradiation for Creating Thermally-Stable High-Resistivity Region in Si CMOS Substrate
Hans Herdian3, Takeshi Inoue1, Takuichi Hirano2, Masatsugu Sogabe1, Atushi Shirane3, Kenichi Okada3
1SHI-ATEX Co., Ltd., Japan; 2Tokyo City University, Japan; 3Tokyo Institute of Technology, Japan

15:24 Impact of Device Shunt Loss on DC-80 GHz SPDT in 22 nm FD-SOI
Martin Rack, L Nyssens, Quentin Courte, Dimitri Lederer, Jean-Pierre Raskin
Université Catholique de Louvain, Belgium

15:36 Novel mmWave NMOS Device for High Pout mmWave Power Amplifiers in 45RF-SOI
Sameer Jain1, Dimitri Lederer2, Arvind Kumar1, Sudesh Saroop1, Chris Prindle1, Purushothaman Srinivasan1, Wen Liu1, Ravi Achanta1, Erdem Kaltalioglu1, Steven Moss1, Paul Colestock1, Greg Freeman1
1GlobalFoundries Inc., United States; 2Université Catholique de Louvain, Belgium
Technical Program: Live interactive sessions with short pitch presentations and Q&A

B1L-6: Memories and 3D Integration (JOINT 2020 TED-brief special edition & SSC-L special edition)

Chair(s): Guilhem Larrieu; Laboratory of Analysis and Architecture of Systems
Alyssa Apsel; Cornell University

Location: CHROME 2
Date: Tuesday, September 14, 15:00 - 16:00

15:00 A 1 Mbit Fully Logic-Compatible 3T Gain-Cell Embedded DRAM in 16nm FinFET
Robert Giterman², Amir Shalom¹, Andreas Burg², Alexander Fish¹, Adam Teman¹
¹Bar-Ilan University, Israel; ²École Polytechnique Fédérale de Lausanne, Switzerland

15:12 Area-Efficient Multi-Hop Inductive Coupling Interface for 3D-Stacked Memory with 0.23-V Transmitter and Sub-10-μm Coil Design
Kota Shiba, Tatsuo Omori, Mototsugu Hamada, Tadahiro Kuroda
University of Tokyo, Japan

15:24 Vertically Replaceable Memory Block Architecture for Stacked DRAM Systems by Wafer-on-Wafer (WOW) Technology
Shinji Sugatani, Norio Chujo, Koji Sakui, Hiroyuki Ryoson, Tomoji Nakamura, Takayuki Ohba
Tokyo Institute of Technology, Institute of Innovative Research, Japan
B2L-1: Machine Learning & In-Memory-Computing with Emerging Technologies

Chair(s): Manuel Le Gallo; IBM Zurich
Thomas Mikolajick; Namlab gGmbH and Technische Universität Dresden

Location: PLATINE Auditorium
Date: Tuesday, September 14, 16:00 - 17:00

16:00 A Maximally Row-Parallel MRAM In-Memory-Computing Macro Addressing Readout Circuit Sensitivity and Area
Peter Deaville, Bonan Zhang, Lung-Yen Chen, Naveen Verma
Princeton University, United States

16:12 A 40nm RRAM Compute-in-Memory Macro Featuring On-Chip Write-Verify and Offset-Cancelling ADC References
Wantong Li, Xiaoyu Sun, Hongwu Jiang, Shanshi Huang, Shimeng Yu
Georgia Institute of Technology, United States

16:24 Low-Overhead Implementation of Binarized Neural Networks Employing Robust 2T2R Resistive RAM Bridges
Mona Ezzadeen1, Atreya Majumdar4, Marc Bocquet1, Bastien Giraud2, Jean-Philippe Noël2, François Andrieu2, Damien Querlioz2, Jean-Michel Portal1
1Aix-Marseille University, Université de Toulon, CNRS, IM2NP, France; 2CEA-List/Leti, Université Grenoble Alpes, France; 3CEA, Aix-Marseille University, Université de Toulon, CNRS, IM2NP, Aix-Marseille University, France; 4Université Paris-Saclay, CNRS, C2N, France

16:36 High-Conductance, Ohmic-Like HfZrO4 Ferroelectric Memristor
Laura Bégon-Lours5, Mattia Halter3, Youri Popoff3, Zhenming Yu4, Donato Francesco Falcone2, Bert Jan Offrein1
1IBM Research GmbH, Switzerland; 2IBM Research, École Polytechnique Fédérale de Lausanne, Switzerland; 3IBM Research, ETH Zürich, Switzerland; 4IBM Research, Institute of Neuroinformatics - Universität Zürich & ETH Zürich, Switzerland; 5National Center for Scientific Research Demokritos / IBM Research, Switzerland

16:48 Emulating Artificial Mechanoreceptor Functionalities from SiO2-Based Memristor and PDMS Stretchable Sensor for Artificial Skin Applications
Panagiotis Bousoulas, Charalampos Papakonstantinopoulos, Dimitris Tsoukalas
National Technical University of Athens, Greece

Chair(s): Denis Rideau; STMicroelectronics
          Viktor Sverdlov; Technische Universität Wien

Location: CHROME 1

Date: Tuesday, September 14, 16:00 - 17:00

16:00 Out-of-Equilibrium Body Potential Measurement on silicon-on-Insulator with Deposited Metal Contacts
Miltiadis Alepidis¹, Aude Bouchard¹, Cecile Delacour², Irina Ionica¹
¹IMEP-LaHC, University Grenoble Alpes, Grenoble-INP and University Saint Mont Blanc, France; ²Neel Institut CNRS, University Grenoble Alpes, France

16:12 Analysis of MIS-HEMT Device Edge Behavior for GaN Technology Using New Differential Method
Roméo Kom Kammeugne¹, Charles Leroux¹, Jacques Cluzel¹, Laura Vauche¹, Cyrille Le Royer¹, Romain Gwoziecki¹, Jérôme Biscarrat¹, Frédéric Xavier Gaillard¹, Matthew Charles¹, Edwige Bano², Gérard Ghibaudo³
¹CEA-Leti, France; ²IMEP-LaHC, University Grenoble Alpes, Grenoble-INP, France; ³IMEP-LaHC, University Grenoble Alpes, University Savoie Mont Blanc, CNRS, Grenoble INP, France

16:24 Characterization and TCAD Modeling of Mixed-Mode Stress Induced by Impact Ionization in Scaled SiGe HBTs
Nicolò Zagni, Francesco Maria Puglisi, Giovanni Verzellesi, Paolo Pavan
Università degli studi di Modena e Reggio Emilia, Italy

16:36 Monte Carlo Comparison of n-Type and p-Type Nanosheets with FinFETs: Effect of the Number of Sheets
Fabian Bufler, Doyoung Jang, Geert Hellings, Geert Ene- man, Philippe Matagne, Alessio Spessot, Myung-Hee Na imec, Belgium
**B2L-6: Energy Efficient Sensor Interfaces**

**Chair(s):** Cédric Tubert; STMicroelectronics  
Matthias Kuhl; Technische Universität Hamburg  

**Location:** CHROME 2  
**Date:** Tuesday, September 14, 16:00 - 17:00

**16:00** An Energy Autonomous Light Intensity Sensor for Monarch Butterfly Migration Tracking  
Yuyang Li¹, Yejoong Kim², Eunseong Moon², Yuxin Gao³, Jamie Phillips¹, Inhee Lee³  
¹University of Delaware, United States; ²University of Michigan, United States; ³University of Pittsburgh, United States

**16:12** A 36V Ultrasonic Driver for Haptic Feedback Using Advanced Charge Recycling Achieving 0.20CV2f Power Consumption  
Jonas Pelgrims³, Kris Myny¹, Wim Dehaene²  
¹imec, Katholieke Universiteit Leuven, Belgium; ²Katholieke Universiteit Leuven, imec, Belgium; ³Katholieke Universiteit Leuven, MICAS, Belgium

**16:24** A Pitch-Matched Analog Front-End with Continuous Time-Gain Compensation for High-Density Ultrasound Transducer Arrays  
Peng Guo¹, Zu-Yao Chang¹, Emile Noothout¹, Hendrik Vos¹, Johan Bosch², Nico de Jong¹, Martin Verweij¹, Michiel Pertijs¹  
¹Delft University of Technology, Netherlands; ²Erasmus MC, Netherlands

**16:36** A 96-Channel 40nm CMOS Fully-Integrated Potentiostat for Electrochemical Monitoring  
Peishuo Li, Tom Molderez, Marian Verhelst  
Katholieke Universiteit Leuven, ESAT-MICAS, Belgium

**16:48** A 0.5 mm² 0.31 V/0.39 V 28 nW/144 nW 65 nm CMOS Solar Cell-Powered Biofuel Cell-Input Biosensing System with PIM/PDM LED Driving for Stand-Alone RF-Less Continuous Glucose Monitoring Contact Lens  
Guowei Chen, Xinyang Yu, Yue Wang, Tran Minh Quan, Naofumi Matsuyama, Takuya Tsujimura, Md. Zahidul Islam, Kiichi Niitsu  
Nagoya University, Japan
**Technical Program: Live interactive sessions with short pitch presentations and Q&A**


Chair(s): Minhao Yang; École Polytechnique Fédérale de Lausanne
Mirjana Banjevic; Sensirion AG

Location: PLATINE Auditorium

Date: Tuesday, September 14, 17:00 - 18:00

**17:00 A Bio-Inspired Reservoir-Computer for Real-Time Stress Detection from ECG Signal**
Sanjeev T Chandrasekaran², Sumukh P Bhanushali², Imon Banerjee¹, Arindam Sanyal²
¹Emory University, United States; ²University at Buffalo, United States

**17:12 Luximos: a 768x64 900-fps Tileable Pipelined X-Ray CMOS Image Sensor for Dental Imaging with 2.6 LSB/nGy Sensitivity**
Nicola Massari³, Xu Hesong², Alessandro Tarolli¹, Luca Parmesan³, Daniele Perenzoni³, Sabrina Colpo¹, Nicola Fronza¹, David Stoppa², Matteo Perenzoni³, Alfredo Maglione¹
¹Advansid, Italy; ²AMS, Switzerland; ³Fondazione Bruno Kessler, Italy

**17:24 A 2.67 μJ Per Measurement FMCW Ultrasound Range-finder System for the Exploration of Enclosed Environments**
Gönenç Berkol, Peter Baltus, Pieter Harpe, Eugenio Cantaore
Eindhoven University of Technology, Netherlands

**17:36 Polarization Independent Band Gaps in CMOS Back-End-of-Line for Monolithic High-Q MEMS Resonator Confinement**
Richard Hudeczek², Peter Baumgartner¹
¹Intel Deutschland, Germany; ²Technical University of Munich, Germany

**17:48 Compact Modeling and Behavioral Simulation of an Optomechanical Sensor in Verilog a**
Houssein Elmi Dawale, Loïc Sibeud, Sébastien Regord, Guillaume Jourdan, Sébastien Rentz, Franck Badets
CEA, France
**Technical Program: Live interactive sessions with short pitch presentations and Q&A**

**B3L-5: Simulation & Modeling for RF & CMOS**

**Chair(s):** Benjamin Iniguez; *University Rovira i Virgili*

Thierry Poiroux; *CEA-Leti*

**Location:** CHROME 1

**Date:** Tuesday, September 14, 17:00 - 18:00

**17:00** Nanoscale InGaAs FinFETs: Band-to-Band Tunneling and Ballistic Transport

Jesus Del Alamo\(^1\), Xiaowei Cai\(^1\), Xin Zhao\(^2\), Alon Vardi\(^2\), Jesus Grajal\(^3\)

\(^1\)Analog Devices Inc., United States; \(^2\)Massachusetts Institute of Technology, United States; \(^3\)Universidad Politécnica de Madrid, Spain

**17:24** Model of Substrate Capacitance of MOSFET RF Switch Inspired by Inverted Microstrip Line

Valentyn Solomko\(^2\), Oguzhan Oezdamar\(^1\), Robert Weigel\(^1\), Amelie Hagelauer\(^3\)

\(^1\)Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany; \(^2\)Infineon Technologies AG, Germany; \(^3\)Universität Bayreuth, Germany

**17:36** Mechanical Band Gap Formation in Anisotropic CMOS Back-End-of-Line Stacks for Monolithic High-Q MEMS Resonator Confinement

Richard Hudeczek\(^2\), Peter Baumgartner\(^1\)

\(^1\)Intel Deutschland, Germany; \(^2\)Technical University of Munich, Germany

**17:48** Operation and Design of Ferroelectric FETs for a BEOL Compatible Device Implementation

Daniel Lizzit, David Esseni

*Università degli Studi di Udine, Italy*
B3L-6: Modelling & Design in Emerging Quantum Computing Technologies

Chair(s): Andrei Vladimirescu; University of California, Berkeley
Adrian Ionescu; École Polytechnique Fédérale de Lausanne

Location: CHROME 2
Date: Tuesday, September 14, 17:00 - 18:00

17:00 Compact Modelling of 22nm FDSOI CMOS Semiconductor Quantum Dot Cryogenic I-V Characteristics
Suyash Pati Tripathi$^2$, Shai Bonen$^2$, Claudia Nastase$^1$, Sergiu Iordănescu$^1$, George Boldeiu$^1$, Mircea Pășteanu$^1$, Alexandru Müller$^1$, Sorin Voinigescu$^2$

$^1$National Institute for Research and Development in Microtechnologies, Romania; $^2$University of Toronto, Canada

17:12 Bias Generation and Calibration of CMOS Charge Qubits at 3.5Kelvin in 22-nm FDSOI
Imran Bashir$^1$, Dirk Leipold$^1$, Mike Asker$^1$, Ali Esmailiyani$^2$, Elena Blokhina$^3$, David Redmond$^2$, Panagiotis Giounanlis$^2$, Dennis Andrade-Miceli$^3$, Robert Bogdan Staszewski$^4$

$^1$Equal1 Labs Inc., United States; $^2$Equal1 NovaUCD, Ireland; $^3$Equal1 NovaUCD, University College Dublin, Ireland; $^4$University College Dublin, Equal1 Labs, NovaUCD, Ireland

17:24 Electronic-Photonic Cryogenic Egress Link
Bozhi Yin$^2$, Hayk Gevorgyan$^1$, Deniz Onural$^1$, Anatol Khilo$^1$, Milos Popović$^1$, Vladimir Stojanović$^2$

$^1$Boston University, United States; $^2$University of California, Berkeley, United States
C1L-1: ESSDERC Keynote 1

Chair(s): Louis Hutin; CEA-Leti
Andreas Burg; École Polytechnique Fédérale de Lausanne

Location: PLATINE Auditorium
Date: Wednesday, September 15, 15:00 - 15:45

15:00 Compute-in-Memory: From Device Innovation to 3D System Integration
Shimeng Yu, Wonbo Shim, Jae Hur, Yuan-Chun Luo, Gihun Choe, Wantong Li, Anni Lu, Xiaochen Peng
Georgia Institute of Technology, United States

C1L-4: ESSDERC Keynote 2

Chair(s): Maud Vinet; CEA-Leti
Nadine Collaert; IMEC

Location: PALLADIUM 2
Date: Wednesday, September 15, 15:00 - 15:45

15:00 Transistors for 100-300GHz Wireless
Mark Rodwell, Brian Markman, Yihao Fang, Logan Whitaker, Hsin-Ying Tseng, Ahmed Ahmed
University of California, Santa Barbara, United States

C3L-1: ESSDERC Keynote 3

Chair(s): Cédric Tubert; STMicroelectronics
Mirjana Banjevic; Sensirion AG

Location: PLATINE Auditorium
Date: Wednesday, September 15, 16:30 - 17:15

16:30 The Essential Contribution of CMOS Imaging Technologies to Earth Observation Applications
Pierre Magnan
ISAE-SupAero, France

On-demand recordings will be available from Friday, September 17
D1L-1: Ultra Low Power Neural Network CMOS Accelerators

Chair(s): Antoine Frappé; Institut Supérieur de l’Électronique et du Numérique
Marian Verhelst; Katholieke Universiteit Leuven

Location: PLATINE Auditorium
Date: Thursday, September 16, 15:00 - 16:00

15:00 A 2.1 pJ/SOP 40nm SNN Accelerator Featuring On-Chip Transfer Learning Using Delta STDP
Ming Ming Wong¹, Sumit Bam Shrestha², Vishnu Paramasivam³, Aarthy Mani³, Yun Kwan Lee³, Eng Kiat Koh³, Wenyu Jiang³, Kevin Tshun Chuan Chai³, Anh Tuan Do¹
¹Agency for Science Technology and Research, Institute of Microelectronics, Singapore; ²Agency for Science, Technology and Research, Institute of Microelectronics, Singapore

15:12 AAD-KWS: A Sub-µW Keyword Spotting Chip with a Zero-Cost, Acoustic Activity Detector from a 170nW MFCC Feature Extractor in 28nm CMOS
Lixuan Zhu, Weiwei Shan, Jiaming Xu, Yicheng Lu
Southeast University, China

15:24 7.5nJ/Inference CMOS Echo State Network for Coronary Heart Disease Prediction
Sanjeev T Chandrasekaran², Imon Banerjee¹, Arindam Sanyal²
¹Emory University, United States; ²University at Buffalo, United States

15:36 A 1.625 TOPS/W SOC for Deep CNN Training and Inference in 28nm CMOS
Yu-Tung Liu¹, Chuking Kung¹, Ming-Hang Hsieh¹, Hsiu-Wen Wang², Chun-Pin Lin², Chao-Yang Yu², Chi-Shi Chen², Tzi-Dar Chiueh¹
¹National Taiwan University, Taiwan; ²Taiwan Semiconductor Research Institute, Taiwan

15:48 A 43pJ Per Inference CBNN-Based Compute-in-Sensor Associative Memory in 28nm FDSOI
Benoit Larras, Antoine Frappé
ISEN-Junia/IEMN, France
Technical Program: Live interactive sessions with short pitch presentations and Q&A

D1L-5: Advanced Devices & Processing

Chair(s): Gianluca Fiori; University of Pisa
Max Lemme; AMO GmbH and RWTH Aachen University

Location: CHROME 1
Date: Thursday, September 16, 15:00 - 16:00

15:00 Complementary Two-Dimensional (2-D) MoS₂ FET Technology
Cristine Jin Estrada, Zichao Ma, Mansun Chan
Hong Kong University of Science and Technology, Hong Kong

15:12 Experimental Assessment of Variability in Junctionless Nanowire nMOS Transistors
Michelly de Souza¹, Sylvain Barraud², Mikaël Cassé¹, Maud Vinet¹, Olivier Faynot¹, Marcelo Pavanello³
¹CEA-Leti, France; ²CEA-Leti, Université Grenoble Alpes, France; ³Centro Universitário da FEI, Brazil

15:24 Improvement on Ge/GeOx/Tm2O3/HfO2 Gate Performance by Forming Gas Anneal
Laura Žurauskaitė, Mikael Östling, Per-Erik Hellström
KTH Royal Institute of Technology, Sweden

15:36 Improving Ge-rich GST ePCM Reliability Through BEOL Engineering
Andrea Redaelli², Anna Gandolfo², Giulia Samanni², Enrico Gomiero², Elisa Petroni², Luca Scotti², Andrea Lippiello², Paolo Mattavelli², Jeremie Jasse², Davide Codegoni², Andrea Serafini², Rossella Ranica², Christian Boccaccio², Juri Sandrini², Remy Berthelon², JC. Grenier², O. Weber², D. Turgis², A. Valery², S. Del Medico², V. Caubet², JP. Reynard², D. Dutartre², L. Favennec², A. Conte², F. Disegni², M. De Tomasi², A. Ventre², M. Baldo¹, D. Ielmini¹, A. Maurelli², P. Ferreira², Franck Arnaud², F. Piazza², Paolo Cappelletti², R. Annunziata³, R. Gonella²
¹Politecnico di Milano, Italy; ²STMicroelectronics, France; ³STMicroelectronics, Italy
**Technical Program: Live interactive sessions with short pitch presentations and Q&A**

**D2L-1: In Memory Computing & Security**

Chair(s): Joachim Rodrigues; *Lund University*
          Damien Querlioz; *Centre for Nanoscience and Nanotechnology and University of Paris-Saclay*

Location: PLATINE Auditorium
Date: Thursday, September 16, 16:00 - 17:00

16:00 **A Calibration-Free In-Memory True Random Number Generator Using Voltage-Controlled MRAM**
Jiyue Yang, Di Wu, Albert Lee, Seyed Armin Razavi, Puneet Gupta, Kang Wang, Sudhakar Pamarti
*University of California, Los Angeles, United States*

16:12 **Exploiting FeFET Switching Stochasticity for Low-Power Reconfigurable Physical Unclonable Function**
Xinrui Guo³, Xiaoyang Ma³, Franz Müller¹, Ricardo Olivo¹, Juejian Wu³, Kai Ni², Thomas Kämpfe¹, Yongpan Liu³, Huazhong Yang³, Xueqing Li³
¹Fraunhofer Institute for Photonic Microsystems, Germany; ²Rochester Institute of Technology, United States; ³Tsinghua University, China

16:24 **A Charge-Domain Computation-in-Memory Macro with Versatile All-Around-Wire-Capacitor for Variable-Precision Computation and Array-Embedded DA/AD Conversions**
Gicheol Shin, Donguk Seo, Jaerok Kim, Johnny Rhe, Eunyoung Lee, Seonho Kim, Soyoun Jeong, Jong Hwan Ko, Yoonmyung Lee
*Sungkyunkwan University, Korea*

16:36 **SRAM with In-Memory Inference and 90% Bitline Activity Reduction for Always-on Sensing with 109 TOPS/mm² and 749-1,459 TOPS/W in 28nm**
Viveka Konandur Rajanna, Sachin Taneja, Massimo Alioto
*National University of Singapore, Singapore*

16:48 **A Zero-Skipping Reconfigurable SRAM In-Memory Computing Macro with Binary-Searching ADC**
Chengshuo Yu², Kevin Tshun Chuan Chai¹, Tony Tae-Hyung Kim², Bongjin Kim²
¹Agency for Science Technology and Research, Institute of Microelectronics, Singapore; ²Nanyang Technological University, Singapore; ³University of California, Santa Barbara, United States
D2L-5: Simulation & Modeling of Defects & Traps

Chair(s): Zlatan Stanojevic; Global TCAD Solutions
Denis Rideau; STMicroelectronics

Location: CHROME 1
Date: Thursday, September 16, 16:00 - 17:00

16:00 Multiscale Modeling Study of Native Oxide Growth on a Si(100) Surface
Lukas Cvitkovich1, Markus Jech1, Dominic Waldhör3, Al-Moatasem Bellah El-Sayed2, Christoph Wilhelmer1, Tibor Grasser1
1Technische Universität Wien, Institute for Microelectronics, Austria; 2Technische Universität Wien, Institute for Microelectronics / Nanolayers Research Computing, Ltd, Austria; 3Technische Universität Wien, Institute for Microelectronics, Christian Doppler Lab., Austria

16:12 Machine Learning Prediction of Defect Structures in Amorphous Silicon Dioxide
Diego Milardovich1, Markus Jech1, Dominic Waldhör3, Al-Moatasem Bellah El-Sayed2, Tibor Grasser1
1Technische Universität Wien, Institute for Microelectronics, Austria; 2Technische Universität Wien, Institute for Microelectronics / Nanolayers Research Computing, Ltd, Austria; 3Technische Universität Wien, Institute for Microelectronics, Christian Doppler Lab., Austria

16:24 Statistical Ab Initio Analysis of Electron Trapping Oxide Defects in the Si/SiO2 Network
Christoph Wilhelmer1, Markus Jech1, Dominic Waldhör3, Al-Moatasem Bellah El-Sayed2, Lukas Cvitkovich1, Tibor Grasser1
1Technische Universität Wien, Institute for Microelectronics, Austria; 2Technische Universität Wien, Institute for Microelectronics / Nanolayers Research Computing, Ltd, Austria; 3Technische Universität Wien, Institute for Microelectronics, Christian Doppler Lab., Austria

16:36 VERILOR: A Verilog-A Model of Lorentzian Spectra for Simulating Trap-Related Noise in CMOS Circuits
Angeliki Tataridou, Gérard Ghibaudo, Christoforos Theodorou
IMEP-LaHC, University Grenoble Alpes, University Savoie Mont Blanc, CNRS, Grenoble INP, France

16:48 Impact of Hot Carrier Degradation on the Performances of Current Mirrors Based on a 55 nm BiCMOS Integrated Circuit Technology
Chhandak Mukherjee3, Marine Couret1, Cristell Maneux1, Didier Céli2
1IMS Laboratory, CNRS UMR 5218, University of Bordeaux, France; 2STMicroelectronics, France; 3Université de Bordeaux, Laboratoire IMS, CNRS UMR 5218, France
D3L-1: In/Near-Memory Computing (JOINT 2020 TEDbrief special edition & SSC-L special edition)

Chair(s): Nitin Chawla; STMicroelectronics
Elisa Vianello; CEA-Leti

Location: PLATINE Auditorium
Date: Thursday, September 16, 17:00 - 18:00

17:00 Ultrahigh-Density 3-D Vertical RRAM with Stacked Junctionless Nanowires for In-Memory-Computing Applications
Mona Ezzadeen, Daphnée Bosch, Bastien Giraud, Sylvain Barraud, Jean-Philippe Noël, Didier Lattard, Joris Lacord, Jean-Michel Portal, François Andrieu
1Aix-Marseille University, Université de Toulon, CNRS, IM2NP, France; 2CEA, France; 3CEA-Leti, Université Grenoble Alpes, France; 4CEA-List/Leti, Université Grenoble Alpes, France; 5CEA, Aix-Marseille University, Université de Toulon, CNRS, IM2NP, Aix-Marseille University, France

17:12 IGZO-Based Compute Cell for Analog In-Memory Computing—DTCO Analysis to Enable Ultralow-Power AI at Edge
Daisuke Saito, Jonas Doevenspeck, Stefan Cosemans, Hyungrock Oh, Manu Perumkunnil, Papistas Ioannis, Belmonte Attilio, Rassoul Nouredine, Delhougne Romain, Kar Gouri, Debacker Peter, Mallik Arindam, Verkest Diederik, Na Nyung-Hee
1imec, Belgium; 2Sony Semiconductor Solutions Corporation, Japan

17:24 A 35.6 TOPS/W/mm2 3-Stage Pipelined Computational SRAM with Adjustable Form Factor for Highly Data-Centric Applications
Jean-Philippe Noël, Manuel Pezzin, Roman Gauchi, Jean-Frédéric Christmann, Maha Kooli, Henri-Pierre Charles, Lorenzo Ciampolini, Mariam Diallo, Florent Lepin, Benjamin Blampey, Pascal Vivet, Subhasish Mitra, Bastien Giraud
1CEA, France; 2CEA-Leti, Université Grenoble Alpes, France; 3CEA-List/Leti, Université Grenoble Alpes, France
D3L-3: Substrates & Design Techniques for RF/mmW Applications (JOINT 2020 TEDbrief special edition & SSC-L special edition)

Chair(s): David Ruffieux; CSEM SA
Jean-Pierre Raskin; Université catholique de Louvain

Location: TITANE 2

Date: Thursday, September 16, 17:00 - 18:00

17:00 Influence of Substrate Resistivity on Porous Silicon Small Signal RF Properties
Geoffroy Godet¹, Emmanuel Augendre¹, Jose Lugo-Alvarrez¹, Hélène Jacquinot¹, Frédéric Xavier Gaillard¹, Thomas Lorne¹, Emmanuel Rolland¹, Thierry Taris², Florence Servant¹
¹CEA-Leti, France; ²IMS Laboratory, IMS Bordeaux, CNRS, France

17:12 Analysis of Gate Metal Resistance in CMOS Compatible RF GaN HEMTs
Rana Elkashlan¹, Raul Rodriguez¹, Sachin Yadav¹, Ahmad Khaled¹, Uthayasakaran Peralagu¹, Alireza Alian¹, Niamh Waldron¹, Ming Zhao¹, Piet Wambacq², Bertrand Parvais¹, Nadine Collaert¹
¹imec, Belgium; ²imec, Vrije Universiteit Brussels, Belgium

17:24 A 108 Gb/S 64-QAM CMOS D-Band Rx with Integrated Lo Generation
Abdelaziz Hamani, Alexandre Siligaris, Cedric Dehos, Nicolas Cassiau, Benjamin Blampey, Fabrice Chaix, Marjorie Gary, José Luis Gonzalez-Jimenez
CEA-Leti, Université Grenoble Alpes, France

17:36 A 84.48Gb/S 64-QAM CMOS D-Band channel-Bonding Tx front-End with Integrated multi-Lo Frequency Generation
Abdelaziz Hamani, Alexandre Siligaris, Fernando Barrera, Cedric Dehos, Nicolas Cassiau, Benjamin Blampey, Fabrice Chaix, Marjorie Gary, José Luis Gonzalez-Jimenez
CEA-Leti, Université Grenoble Alpes, France; CEA-Leti, Université Grenoble Alpes, Finland
Technical Program: Live interactive sessions with short pitch presentations and Q&A

D3L-5: Simulation & Modeling for Memory & Imaging Applications

Chair(s): Wladek Grabinski; MOS-AK Association
Viktor Sverdlov; Technische Universität Wien

Location: CHROME 1
Date: Thursday, September 16, 17:00 - 18:00

17:00 Polarization Switching and Interface Charges in BEOL Compatible Ferroelectric Tunnel Junctions
Riccardo Fontanini¹, Justine Barbot¹, Mattia Segatto⁴, Suzanne Lancaster², Quang Duong³, Francesco Driussi⁴, Laurent Grenouillet¹, François Triozon¹, Jean Coignus¹, Thomas Mikolajick³, Stefan Slesazeck², David Esseni⁴
¹CEA-Leti, France; ²NaMLab gGmbH, Germany; ³Technische Universität Dresden, Institute for Semiconductor & Microsystems Technology, NaMLab gGmbH, Germany; ⁴Università degli Studi di Udine, Italy

17:12 Fast Behavioral VerilogA Compact Model for Stochastic MTJ
Etienne Becle, Philippe Talatchian, Guillaume Prenat, Lorena Anghel, Ioan-Lucian Prejbeanu
CEA-Spintec, France

17:24 A Fokker-Planck Solver to Model MTJ Stochasticity
Fernando García-Redondo, Pranay Prabhat, Mudit Bhargava
Arm Ltd., United States; Arm Ltd., United Kingdom

17:36 Semi-Empirical Model for Optical Properties of Si₁−xGex Alloys Accounting for Strain and Temperature
Jérémy Grebot¹, Gabriel Mugny², Rémi Helleboid², Isobel Nicholson², Francesco Abbate², Denis Rideau², Claire Scheid⁴, Stéphane Lanteri¹, Hélène Wehbe-Alaou²
¹INRIA Sophia-Antipolis, France; ²STMicroelectronics, France; ³STMicroelectronics, United Kingdom; ⁴STMicroelectronics, INRIA Sophia-Antipolis, France; ⁵Université de Nice, France

17:48 Comprehensive Modeling and Characterization of Photon Detection Efficiency and Jitter in Advanced SPAD Devices
Rémi Helleboid², Denis Rideau², Isobel Nicholson², Norbert Moussy¹, Olivier Saxod¹, Marie Basset², Jérémy Grebot³, Antonin Zimmerman², Bastien Mamdý², Dominik Golanski², Megan Agnew², Sara Pellegrini², Mathieu Sicre²
¹CEA-Leti, France; ²STMicroelectronics, France; ³STMicroelectronics, United Kingdom; ⁴STMicroelectronics, INRIA Sophia-Antipolis, France
D3L-6: Emerging Sensor Technologies

Chair(s): Francis Calmon; Institut National des Sciences Appliquées de Lyon
Radu Sporea; University of Surrey

Location: CHROME 2
Date: Thursday, September 16, 17:00 - 18:00

17:00 Wafer-Scale Fabrication of Biologically Sensitive Si Nanowire FET: From pH Sensing to Electrical Detection of DNA Hybridization
Rony Midahuen¹, Bernard Previtali¹, Caroline Fontelaye¹, Guillaume Nonglaton¹, Valérie Stambouli-Sene², Sylvain Barraud¹
¹CEA-Leti, Université Grenoble Alpes, France; ²Université Grenoble Alpes, CNRS, Grenoble-INP, LMGP, France

17:12 Design and Fabrication of a Ring-Coupled Mach-Zehnder Interferometer Gyroscope
Eva Kempf³, Pierre Labeye¹, Philippe Grosse¹, Frédéric Bœuf³, Stéphane Monfray³, Paul Charette⁴, Régis Orobtchouk²
¹CEA Grenoble, France; ²Institut des Nanotechnologies de Lyon, INSA Lyon, France; ³STMicroelectronics, France; ⁴Université de Sherbrooke, Laboratoire Nanotechnologies et Nanosystèmes, Canada

17:24 High Tuning Range Spiking 1R-1T VO2 Voltage-Controlled Oscillator for Integrated RF and Optical Sensing
Teodor Rosca, Fatemeh Qaderi, Adrian Mihai Ionescu
École Polytechnique Fédérale de Lausanne, Switzerland

ESSCIRC ESSDERC 2021 SSCS/EDS Joint YP and WiC mentoring and networking event

Location: Palladium 2
Date: Thursday, September 16, 17:00-18:00

The IEEE Solid-State Circuits Society (SSCS) Women in Circuits and Young Professionals and the IEEE Electron Devices Society (EDS) are happy to host a virtual mentoring session in conjunction with ESSCIRC ESSDERC 2021. After a short kickoff from a renowned engineer in our field, you can choose to join a breakout room with mentors who will speak on a variety of topics. Topics include: Mentoring and Networking in a virtual world, a career in industry/startups, becoming a professor, leading a technical team to success, the how-to for virtual job search, and more.
E1L-1: Cryogenic Electronics for Quantum Computing

Chair(s): Louis Hutin; CEA-Leti
Claudio Bruschini; École Polytechnique Fédérale de Lausanne

Location: PLATINE Auditorium
Date: Friday, September 17, 15:00 - 16:00

15:00 Performance Trade-Off Scenarios for GAA Nanosheet FETs Considering Inner-Spacers and Epi-Induced Stress: Understanding & Mitigating Process Risks
Amita Rawat1, Krishna Bhuwalka1, Philippe Matagne2, Bjorn Vermersch2, Hao Wu1, Geert Hellings2, Julien Ryckaert2, Changze Liu1
1Huawei Technologies Research & Development, Belgium; 2imec, Belgium

15:12 Electric-Field Controlled Spin Transport in Bilayer CrI3
Damiano Marian2, David Soriano2, Enrique G. Marin1, Giuseppe Iannaccone2, Gianluca Fiori2
1Universidad de Granada, Spain; 2Università di Pisa, Italy

15:24 Circuit Model for the Efficient Co-Simulation of Spin Qubits and Their Control & Readout Circuitry
Benjamin Gys2, Fahd Ayyalil Mohiyaddin1, Rohith Acharya2, Roy Li1, Kristiaan De Greve1, Georges Gielen3, Bogdan Govoreanu1, Iuliana Radu1, Francky Catthoor2
1imec, Belgium; 2imec, Katholieke Universiteit Leuven, Belgium; 3Katholieke Universiteit Leuven, imec, Belgium

15:36 Cryogenic Characterization and Modeling of 14 nm Bulk FinFET Technology
Asma Chabane, Mridula Prathapan, Peter Mueller, Eunjung Cha, Pier Andrea Francese, Marcel Kossel, Thomas Morf, Cezar Zota
IBM Research GmbH, Switzerland

15:48 Cryogenic Characterization of 16 nm FinFET Technology for Quantum Computing
Hung-Chi Han1, Farzan Jazaeri1, Antonio D'Amico1, Andrea Baschiotto3, Edoardo Charbon1, Christian Enz2
1École Polytechnique Fédérale de Lausanne, Switzerland; 2École Polytechnique Fédérale de Lausanne, Integrated Circuits Laboratory, Switzerland; 3Università degli Studi di Milano-Bicocca, Italy
E1L-5: Advanced Memory Devices

Chair(s): Qing-Tai Zhao; Forschungszentrum Jülich
Tortorelli Innocenzo; Micron Technologies

Location: CHROME 1
Date: Friday, September 17, 15:00 - 16:00

15:00 Enhanced Data Integrity of In-Ga-Zn-Oxide Based Capacitor-Less 2T Memory for DRAM Applications
Hyungrock Oh¹, Attilio Belmonte¹, Manu Perumkunnil¹, Jerome Mitard¹, Nouredine Rassoul¹, Gabriele Luca Donadio¹, Romain Delhougne¹, Arnaud Furnemont¹, Gouri Sankar Kar¹, Wim Dehaene²
¹imec, Belgium; ²Katholieke Universiteit Leuven, imec, Belgium

15:12 Vertical and Lateral Charge Losses During Short Time Retention in 3-D NAND Flash Memory
Yongwoo Lee¹, Jinsu Yoon¹, Kwangmin Lim², Bongsik Choi², Geon-Hwi Park¹, Ju Won Jeon¹, Jong-Ho Bae¹, Dong Myong Kim¹, Dae Hwan Kim¹, Eunmee Kwon², Sung-Jin Choi¹
¹Kookmin University, Korea; ²SK Hynix Semiconductor Inc., Korea

15:24 Layout-Based Evaluation of Read/Write Performance of SOT-MRAM and SOTFET-RAM
Olalekan Afuye, Shady Agwa, Christopher Batten, Alyssa Apsel
Cornell University, United States

15:36 Scaling Ferroelectric HZO Thickness for Low Power GeMFS-FTJ Memories
Nikitas Siannas¹, Christina Zacharaki¹, Polychronis Tsipas¹, Stefanos Chaitoglou¹, Laura Bégon-Lours², Athanasios Dimoulas¹
¹National Center for Scientific Research Demokritos, Greece; ²National Center for Scientific Research Demokritos / IBM Research, Greece

15:48 4-Terminal Ferroelectric Schottky Barrier Field Effect Transistors as Artificial Synapses
Fengben Xi, Han Yi, Andreas Tiedemann, Detlev Grützmacher, Qing-Tai Zhao
Forschungszentrum Jülich GmbH, Germany
E2L-1: Cryogenic Electronics (JOINT 2020 TEDbrief special edition & SSC-L special edition)

Chair(s): Sorin Voinigescu; University of Toronto
David Esseni; University of Udine

Location: PLATINE Auditorium
Date: Friday, September 17, 16:00 - 17:00

16:00 Cryogenic Operation of Thin-Film FDSOI nMOS Transistors: the Effect of Back Bias on Drain Current and Transconductance
Mikaël Cassé², Bruna Cardoso Paz³, Gérard Ghibaudo⁵, Thierry Poiroux², Sylvain Barraud³, Maud Vinet², de Franceschi Silvano¹, Tristan Meunier⁴, Frédéric Xavier Gaillard²
¹CEA-IRIG, France; ²CEA-Leti, France; ³CEA-Leti, Université Grenoble Alpes, France; ⁴CNRS Institut Néel, France; ⁵IMEP-LaHC, University Grenoble Alpes, University Savoie Mont Blanc, CNRS, Grenoble INP, France

16:12 Performance and Low-Frequency Noise of 22-nm FDSOI Down to 4.2 K for Cryogenic Applications
Bruna Cardoso Paz³, Mikaël Cassé², Christoforos Theodorou⁶, Gérard Ghibaudo⁵, Thorsten Kammler⁶, Luca Pirro⁵, Maud Vinet², Silvano de Franceschi¹, Tristan Meunier⁴, Frédéric Xavier Gaillard²
¹CEA-IRIG, France; ²CEA-Leti, France; ³CEA-Leti, Université Grenoble Alpes, France; ⁴CNRS Institut Néel, France; ⁵GlobalFoundries Inc., Germany; ⁶IMEP-LaHC, University Grenoble Alpes, University Savoie Mont Blanc, CNRS, Grenoble INP, France

16:24 A Cryo-CMOS Digital Cell Library for Quantum Computing Applications
Edwin Schriek³, Fabio Sebastiano¹, Edoardo Charbon²
¹Delft University of Technology, Netherlands; ²École Polytechnique Fédérale de Lausanne, Switzerland; ³Independent, Netherlands

16:36 Bias Voltage DAC Operating at Cryogenic Temperatures for Solid-State Qubit Applications
Patrick Vliex¹, Carsten Degenhardt¹, Christian Grewing¹, Dennis Nielinger¹, Stefan van Waasen¹, Stefan Heinen²
¹Forschungszentrum Jülich GmbH, Germany; ²RWTH Aachen University, Germany
Technical Program: Live interactive sessions with short pitch presentations and Q&A

E2L-5: GaN Technology & Characterization

Chair(s): Nadine Collaert; IMEC
Christoforos Theodorou; IMEP-LAHC Grenoble INP

Location: CHROME 1

Date: Friday, September 17, 16:00 - 17:00

16:00 Reliable Method for Low Field Temperature Dependent Mobility Extraction at Al2O3/GaN Interface

1CEA-Leti, France; 2CEA-Leti, Université Grenoble Alpes, IMEP-LAHC MINATEC, France; 3CEA-Leti, Université Grenoble Alpes, IMEP-LAHC MINATEC, University of Padova, France; 4IMEP-LaHC, University Grenoble Alpes, University Savoie Mont Blanc, CNRS, Grenoble INP, France; 5STMicroelectronics, Italy

16:12 Parasitic Capacitance Analysis in Short Channel GaN MIS-HEMTs
Roméo Kom Kammeugne, Charles Leroux, Tadeu Mota Frutuoso, Jacques Cluzel, Laura Vauche, Cyrille Le Royer, Romain Gwoziecki, Xavier Garros, Frédéric Xavier Gaillard, Matthew Charles, Edwige Bano, Gérard Ghibaudo

1CEA-Leti, France; 2IMEP-LaHC, University Grenoble Alpes, Grenoble-INP, France; 3IMEP-LaHC, University Grenoble Alpes, University Savoie Mont Blanc, CNRS, Grenoble INP, France

16:24 Impact of III-N Buffer Layers on RF Losses and Harmonic Distortion of GaN-on-Si Substrates
Pieter Cardinael, Sachin Yadav, Ming Zhao, Martin Rack, Dimitri Lederer, Nadine Collaert, Bertrand Parvais, Jean-Pierre Raskin

1imec, Belgium; 2Université Catholique de Louvain, Belgium

16:36 Integration and Reliability Aspects of Low-Temperature and Au-Free Ta/Al-Based Ohmic Contacts for AlGaN/ GaN MIS-HEMTs
Anthony Calzolaro, Thomas Mikolajick, Andre Wachowiak

1Dresden University of Technology, NaMLab gGmbH, Germany; 2NaMLab gGmbH, Germany; 3Technische Universität Dresden, Institute for Semiconductor & Microsystems Technology, NaMLab gGmbH, Germany
E3L-5: Device Modelling (2020 TEDbrief special edition)

Chair(s): Cristell Maneux; University of Bordeaux
Thierry Poiroux; CEA-Leti

Location: CHROME 1
Date: Friday, September 17, 17:00 - 18:00

17:00 Conductance in a Nanoribbon of Topologically Insulating MoS2 in the 1T' Phase
Viktor Sverdlov\(^1\), Al-Moatasem Bellah El-Sayed\(^3\), Hans Kossina\(^2\), Siegfried Selberherr\(^2\)
\(^1\)Technische Universität Wien, CDL for NovoMemLog, IuE, Austria; \(^2\)Technische Universität Wien, Institute for Microelectronics, Austria; \(^3\)Technische Universität Wien, Institute for Microelectronics / Nanolayers Research Computing, Ltd, Austria

17:12 Analytical Model for Interface Traps Dependent Back Bias Capability and Variability in Ultrathin Body and Box FDSOI MOSFETs
Wangyong Chen, Linlin Cai, Xiaoyan Liu, Gang Du
Peking University, China

17:24 Charge-Based Model for the Drain-Current Variability in Organic Thin-Film Transistors Due to Carrier-Number and Correlated-Mobility Fluctuation
Aristeidis Nikolaou\(^1\), Ghader Darbandy\(^3\), Jakob Leise\(^3\), Jakob Pruefer\(^3\), James W. Borchert\(^1\), Michael Geiger\(^1\), Hagen Klauk\(^1\), Benjamin Iñiguez\(^2\), Alexander Kloes\(^3\)
\(^1\)Max Planck Institute for Solid State Research, Germany; \(^2\)Universitat Rovira i Virgili, Spain; \(^3\)University of Applied Sciences Mittelhessen, Germany

17:36 Macromodel for AC and Transient Simulations of Organic Thin-Film Transistor Circuits Including Nonquasistatic Effects
Jakob Leise\(^3\), Jakob Pruefer\(^3\), Aristeidis Nikolaou\(^3\), Ghader Darbandy\(^3\), Hagen Klauk\(^1\), Benjamin Iñiguez\(^2\), Alexander Kloes\(^3\)
\(^1\)Max Planck Institute for Solid State Research, Germany; \(^2\)Universitat Rovira i Virgili, Spain; \(^3\)University of Applied Sciences Mittelhessen, Germany
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